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FOLEY AND LARDNER LLP
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/800,631	NAKAMURA, AKIHISA	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 7-11, and new claim 12 have been considered. Claims 4-6 have been cancelled as per Applicants' request. Claims 1, 7, and 11 have been amended as per Applicants' request. New claim 12 has been added as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 01 October 2007.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7-9, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kucukcakar et al., U.S. Patent Number 6,138,229 (herein referred to as Kucukcakar) in view of Ing-Simmons et al., U.S. Patent Number 5,239,654 (herein referred to as Ing-Simmons).

5. Referring to claims 1 and 11, taking claim 1 as exemplary, Kucukcakar has taught a processor system comprising:

a. A fixed processing unit having a predetermined information processing function (Kucukcakar Abstract "...The instruction execution unit (**34**) has a non-programmable section (**46**)..."; column 2, lines 25-41 "...Datapath **16** has both a non-programmable data path **18** and a programmable datapath **32**..."; Figure 1; Figure 2; and Figure 3);

b. A variable processing unit having a variable information processing function (Kucukcakar Abstract "...The instruction execution unit (**34**) has...a programmable section (**48**)..."; column 2, lines 25-41 "...Datapath **16** has both a non-programmable data path **18** and a programmable datapath **32**..."; Figure 1; Figure 2; and Figure 3);

c. A control unit which controls so as to cause the fixed processing unit to process a provided task, or so as to cause the variable processing unit to process the task after newly setting an information processing function of the variable processing unit (Kucukcakar column 2, line 42 to column 3, line 25 "...Opcode values are received by a controller or instruction execution unit **34**..."; column 4, lines 36-55 "...transferred via selector logic circuit **49** to CONTROL BUS **15** for controlling datapath **16**..."; Figure 1; Figure 2; and Figure 3);

6. Kucukcakar has not taught

a. A plurality of co-processors;

b. A main processor which preferentially processes the task;

c. An arbitrating unit which analyzes the task, and allocates the task to said plurality of co-processors in accordance with a result of the analysis;

d. Wherein the fixed processing unit and the variable processing unit are provided as a plurality of sets in accordance with a plurality of image signals, and respectively process said plurality of image signals in parallel, and

e. Wherein the arbitrating unit analyzes the task, and in accordance with a result of the analysis, determines whether the task is allocated to only the main processor or the task is allocated to the main processor and said plurality of co-processors.

7. However, Kucukcakar has taught a DSP (Kucukcakar column 1, lines 33-43 "...DSP processors have circuitry to handle such tasks as complex mathematical processing and video image generation...") which processes images, but not the exact layout of the entire chip, just the specifics of a processor's datapath. Ing-Simmons has taught

a. A plurality of co-processors (Ing-Simmons column 1, line 51 to column 2, line 17 "...Such imaging systems are prime candidates for multi-processing where different processors perform different tasks concurrently in parallel..."; column 2, line 54 to column 3, line 2 "...designing a multi-processing system to handle image processing and graphics...when the processors are operating in the MIMD mode. When the processors are running in the SIMD mode..."; column 62, line 21 to column 63, line 13 "...embodiment of the system which is the subject of this invention..."; Figure 61; Figure 62; Figure 63; and Figure 64);

b. A main processor which preferentially processes the task (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-103** and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; Figure 1; and Figure 4);

c. An arbitrating unit which analyzes the task, and allocates the task to said plurality of co-processors in accordance with a result of the analysis (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-103** and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; Figure 1; and Figure 4);

d. Wherein the fixed processing unit and the variable processing unit are provided as a plurality of sets in accordance with a plurality of image signals, and respectively process said plurality of image signals in parallel (Ing-Simmons column 1, line 51 to column 2, line 17 "...Such imaging systems are prime candidates for multi-processing where different processors perform different tasks concurrently in parallel..."; column 2, line 54 to column 3, line 2 "...designing a multi-processing system to handle image processing and graphics...when the processors are operating in the MIMD mode. When the processors are running in the SIMD mode..."; column 62, line 21 to column 63, line 13 "...embodiment of the system which is the subject of this invention..."; Figure 61; Figure 62; Figure 63; and Figure 64), and

e. Wherein the arbitrating unit analyzes the task, and in accordance with a result of the analysis, determines whether the task is allocated to only the main processor or the task is allocated to the main processor and said plurality of co-processors (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-**

103 and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; Figure 1; and Figure 4 – In regards to Ing-Simmons, the Master processor receives all instructions and controls transferring and scheduling accordingly, including which processor, itself or one of the other co-processors, executes which instruction.).

8. In regards to Kucukcakar in view of Ing-Simmons, Kucukcakar only teaches the details of a specific datapath within a processor, but not the details of the entire processing system. Ing-Simmons has taught the details of the entire processing system, such as those shown in Figures 61-64, without the details of the datapath and why a person of ordinary skill in the art at the time the invention was made would want to use the entire system. A person of ordinary skill in the art at the time the invention was made, and as taught by Kucukcakar, would have recognized that the SIMD/MIMD structure allows a very high degree of flexibility to satisfy constantly changing criteria (Kucukcakar column 2, lines 32-41 "...The architecture must allow a very high degree of flexibility..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the SIMD/MIMD architecture of Kucukcakar in the device of Ing-Simmons to increase flexibility of the system.

9. Claim 11 has similar limitations to claim 1 and is rejected for similar reasons. The only difference is claim 11 is for a method while claim 1 is for a processor.

10. Referring to claim 2, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the control unit analyzes the provided task, and controls so as to cause the variable processing unit to process the task after newly setting an information processing function of the variable processing unit in accordance with a result of the analysis (Kucukcakar column 2, line 42 to column 3, line 25 "...Opcode values are received by a controller or instruction execution unit **34**..."; column 3, lines 48-67 "...Selector logic circuit **49** selects either the control signals from non-programmable section **46** or programmable section **48** for transfer to datapath **16**..."; column 4, lines 36-55 "...transferred via selector logic circuit **49** to CONTROL BUS **15** for controlling datapath **16**..."; Figure 1; Figure 2; and Figure 3).

11. Referring to claim 3, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the variable processing unit has at least one of an ALU, a MAC, a LUT, and a FIFO (Kucukcakar column 4, lines 49-55 "...the logic gates in programmable datapath **32** can be configured to function as...an Arithmetic Logic Unit (ALU)..."; Figure 1, Figure 2, and Figure 3), and realizes a new information processing function in accordance with connection information provided from the control unit (Kucukcakar column 2, line 42 to column 3, line 25 "...Opcode values are received by a controller or instruction execution unit **34**..."; column 4, lines 36-55 "...transferred via selector logic circuit **49** to CONTROL BUS **15** for controlling datapath **16**..."; Figure 1; Figure 2; and Figure 3).

12. Referring to claim 7, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the arbitrating unit calculates a processing time in a case of analyzing and processing the task by only the main processor, and on the basis of the calculated time, determines whether or not the task is processed by only the main processor (Kucukcakar

Abstract "...processor (**10**) implements complex, time-consuming operations..." and column 2, lines 12-24 "...processor implements complex, time-consuming operations..." and Ing-Simmons column 9, line 10 to column 10, line 7 "...The operation characteristic of a SIMD operation is that at any period of time a relatively small amount of the data with respect to the entire image is being operated on...").

13. Referring to claim 8, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the variable processing unit has a function of carrying out filtering processing on image information to be provided (Ing-Simmons column 1, line 51 to column 2, line 17 "...Such imaging systems are prime candidates for multi-processing where different processors perform different tasks concurrently in parallel..."; column 2, line 54 to column 3, line 2 "...designing a multi-processing system to handle image processing and graphics..."; column 9, line 10 to column 10, line 7 "...The operation characteristic of a SIMD operation is that at any period of time a relatively small amount of the data with respect to the entire image is being operated on..."; column 62, line 21 to column 63, line 13 "...embodiment of the system which is the subject of this invention..."; Figure 61; Figure 62; Figure 63; and Figure 64).

14. Referring to claim 9, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the variable processing unit has a function of carrying out identification processing on image information to be provided (Ing-Simmons column 1, line 51 to column 2, line 17 "...Such imaging systems are prime candidates for multi-processing where different processors perform different tasks concurrently in parallel..."; column 2, line 54 to column 3, line 2 "...designing a multi-processing system to handle image processing and

graphics..."; column 9, line 10 to column 10, line 7 "...The operation characteristic of a SIMD operation is that at any period of time a relatively small amount of the data with respect to the entire image is being operated on..."; column 62, line 21 to column 63, line 13 "...embodiment of the system which is the subject of this invention..."; Figure 61; Figure 62; Figure 63; and Figure 64).

15. Referring to claim 12, Kucukcakar in view of Ing-Simmons has taught the processor system according to claim 1, wherein the arbitrating unit comprises:

a. A direct memory access unit (Ing-Simmons column 13, lines 16-40 "Transfer processor **11**...transfers data between external memory and the various internal memory elements..." and Figure 57– In regards to Ing-Simmons, the transfer processor functions similarly to a direct memory access (DMA) unit.);

b. A program analyzer that receives a processing program (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-103** and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; Figure 1; and Figure 4);

c. A memory connected to the program analyzer (Ing-Simmons column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**..."; Figure 1; and Figure 4);

d. An operating program storage unit that stores an operating program therein (Ing-Simmons column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**..."; Figure 1; and Figure 4 – In

regards to Ing-Simmons, the memory 10 shown in Figure 4 includes instruction memory, which holds the programs instructions being executed.);

e. A setting register that stores register information corresponding to connection information (Ing-Simmons column 20, line 48 to column 21, line 10 "...register **2100-2103**...for indicating if synchronized operation is required..."; column 27, line 26 to column 28, line 14 "...Register 2820 contains the current operating mode of the system..."; Figure 21; Figure 22; and Figure 28);

f. A data address control unit that transmits and receives data and addresses (Ing-Simmons column 39, lines 26-56 "Address unit **3001**..."; Figure 30; and Figure 32);

g. An interruption control unit that receives an respective interruption signal corresponding to an operating state of each of the plurality of co-processors (Ing-Simmons column 45, line 8 to column 46, line 35 "...there is a global interrupt enable bit..."; column 46, line 48 to column 47, line 7 "...In SIMD configuration there is also the need to pass back to the "master" PP 100 to the "slave" PPs 101-103 that indicates that it is taking an interrupt..."; Figure 30; and Figure 31); and

h. A main processor/co-processor control unit that receives the respective interruption signal from the interruption control unit and determines which of the plurality of coprocessors are currently capable of executing the task (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-103** and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; column 51, lines 38-58 "...Once

an enabled interrupt is detected, the sequence of pseudo-instructions is commenced..."; Figure 1; Figure 4; and Figure 39),

i. Wherein the arbitrating unit carries out allocation of the task in accordance with a processing function or a processor speed and the determination of the main processor/coprocessor control unit (Ing-Simmons column 6, lines 5-19 "...there is a set of parallel processors **100-103** and a master processor **12**..."; column 6, line 59 to column 7, line 43 "...master processor **12** is shown connected to the memories via crossbar switch **20**. Transfer processor **11**..."; column 13, line 14 to column 15, line 5 "...The master processor...is used for scheduling and control of the entire system..."; Figure 1; and Figure 4).

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kucukcakar et al., U.S. Patent Number 6,138,229 (herein referred to as Kucukcakar) in view of Ing-Simmons et al., U.S. Patent Number 5,239,654 (herein referred to as Ing-Simmons), as applied to claim 1 above, and further in view of Sasaki et al., U.S. Patent Number 4,758,885 (herein referred to as Sasaki). Kucukcakar in view of Ing-Simmons has not explicitly taught the processor system according to claim 1, wherein the variable processing unit has a function of carrying out color conversion processing on image information to be provided. However, Kucukcakar has taught processing images (Kucukcakar column 1, lines 33-43 "...DSP processors have circuitry to handle such tasks as complex mathematical processing and video image generation..."). A person of ordinary skill in the art at the time the invention was made, and as taught by Sasaki, would have recognized that the color image processing of Sasaki obtains a high quality color image from various input systems (Sasaki column 1, line 65 to column 2, line 11 "...the color

reproducing ranges of the input and output systems differ as well, a high quality image can be reproduced...obtain a high quality color image..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the color processing of Sasaki in the device of Kucukcakar to improve image quality.

Response to Arguments

17. Applicant's arguments filed 01 October 2007 have been fully considered but they are not persuasive.

18. The Examiner notes that the arguments in general argue the references separately, as would be proper if the limitations were previously rejected using a single reference. However, the claim limitations argued were moved into the independent claims from dependent claims previously rejected under the combination of Kucukcakar in view of Ing-Simmons. As such, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

19. Applicant's argue in essence on pages 5-6

> ...The system of Kucukcakar et al. does not have a plurality of co-processors, each having a fixed processing unit and a variable processing unit. Nor does it have an arbitrating unit, which analyzes a task and allocates the task to a plurality of co-processors in accordance with a result of the analysis...

20. This has not been found persuasive. As stated in the previous rejection and the rejection above, Kucukcakar was not relied upon to teach the co-processors or arbitrating unit. Ing-

Simmons was relied upon to teach these elements. Kucukcakar only teaches the details of a specific datapath within a single processor, but not the details of the entire image processing system. Ing-Simmons has taught the details of an entire image processing system, such as those shown in Figures 61-64, without the details of the datapath and why a person of ordinary skill in the art at the time the invention was made would want to use the entire image system.

21. Applicants' argue in essence on page 6

> ...While Ing-Simmons' master processor is used to schedule and control the entire system, it does not teach or suggest that the master processor determines whether a task is to be allocated to only the main processor or whether the task is to be allocated to the main processor and the plurality of processors...Ing-Simmons's master processor only performs scheduling for the processors on the crossbar switch, and whereby Ing-Simmons' master processor does not itself execute any tasks.

22. This has not been found persuasive. Ing-Simmons in column 13, line 43 to column 14, line 15 teaches that the Master Processor decides whether a parallel processor or itself executes a particular instruction. Ing-Simmons further teaches that there are certain operations, such as those found above the line in Figure 11, that would preferentially be executed on the Master Processor, since the Master Processor is better suited to executing these functions. However, this designation is arbitrary and based on the processors types of the Master and other parallel processors. Ing-Simmons further explains in column 15, line 62 to column 16, line 6 that the operations below the line in Figure 11 are more efficiently performed in SIMD mode, since they

require more processing, while the operations above the line require less processing and can be performed by a single processor.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

15 December 2007